CLAIMS

1. A method of forming a relaxed graded semiconductor layer on a substrate, the method comprising the steps of:

providing a first semiconductor layer; and

epitaxially growing over the first semiconductor layer a relaxed graded layer comprising at least one of silicon and germanium, with increasing germanium content at a gradient exceeding about 25% Ge/μm to a final composition having a germanium content ranging from greater than 0% to 100% and a threading dislocation density not exceeding about $10^7/cm^2$.

2. The method of claim 1 wherein the graded layer has a dislocation pile-up density not exceeding about 20/cm.

3. The method of claim 1 wherein the graded layer has a dislocation pile-up density not exceeding about 1/cm.

4. The method of claim 1 wherein the graded layer has a dislocation pile-up density not exceeding about 0.01/cm.

5. The method of claim 1 wherein the grading rate is at least 30% Ge/μm.

6. The method of claim 1 wherein the grading rate is at least 40% Ge/μm.

7. The method of claim 1 wherein the epitaxial growth occurs at a temperature ranging from 900 - 1200 °C.

8. The method of claim 7 wherein the epitaxial growth occurs at a rate greater than about 1 nm/s.

9. The method of claim 1 wherein the relaxed graded layer has a thickness ranging from 0.1 to 4.0 μm.

10. The method of claim 1 wherein the first semiconductor has a plurality of threading dislocations distributed substantially uniformly across a surface thereof, and further comprising the step of providing a compositionally uniform cap layer over the surface of the first layer, the cap layer being substantially relaxed, the relaxed graded layer being grown over the cap layer.

11. The method of claim 10 wherein a lattice constant of the compositionally uniform cap layer is different from a lattice constant of the first layer.

12. A semiconductor structure comprising a first semiconductor layer and, thereover, a relaxed graded epitaxial layer comprising silicon and germanium and graded with increasing germanium content at a gradient exceeding 25% Ge/μm to a final composition having a germanium content ranging from greater than 0% to 100%, wherein the structure has a threading dislocation density not exceeding $10^7/cm^2$.

13. The structure of claim 12 wherein the dislocation pile-up density does not exceed 1/cm.

14. The structure of claim 12 wherein the dislocation pile-up density does not exceed 0.01/cm.

15. The structure of claim 12 wherein the relaxed graded layer is graded at a rate of at least 30% Ge/μm.

16. The structure of claim 12 wherein the relaxed graded layer is graded at a rate of at least 40% Ge/μm.

17. The structure of claim 12 wherein the relaxed graded layer has a thickness ranging from 0.1 to 4.0 μm.

18. The structure of claim 12 wherein the first semiconductor layer has a plurality of threading dislocations distributed substantially uniformly across a surface thereof, and further comprising the step of providing a compositionally uniform cap layer over the surface of the first layer, the cap layer being substantially relaxed and having a lattice constant different from a lattice constant of the first layer, the relaxed graded layer being disposed over the cap layer.

19. A semiconductor structure comprising:

a first semiconductor layer and, thereover, a relaxed graded epitaxial layer comprising silicon and germanium and graded with increasing germanium content at a gradient exceeding 25% Ge/μm to a final composition having a germanium content ranging from greater than 0% to 100%, wherein the structure has a threading dislocation density not exceeding $10^7/cm^2$;

a relaxed compositionally uniform cap layer disposed over the graded layer; and

a p-type metal-oxide-semiconductor (PMOS) transistor disposed over the relaxed cap layer, the PMOS transistor including:

a gate dielectric portion disposed over a portion of the relaxed cap layer,

a gate disposed over the gate dielectric portion, the gate comprising a conducting layer, and

a source and a drain disposed proximate the gate dielectric portion, the source and first drain including p-type dopants.

20. A semiconductor structure comprising:

a first semiconductor layer and, thereover, a relaxed graded epitaxial layer comprising silicon and germanium and graded with increasing germanium content at a gradient exceeding 25% Ge/μm to a final composition having a germanium

content ranging from greater than 0% to 100%, wherein the structure has a threading dislocation density not exceeding $10^7/cm^2$;

a relaxed compositionally uniform cap layer disposed over the graded layer; and

an n-type metal-oxide-semiconductor (NMOS) transistor disposed over the relaxed cap layer, the NMOS transistor including:

a gate dielectric portion disposed over a portion of the relaxed cap layer,

a gate disposed over the gate dielectric portion, the gate comprising a conducting layer,

a source and a drain disposed proximate the gate dielectric portion, the source and drain including n-type dopants.

21. A semiconductor structure comprising:

a first semiconductor layer and, thereover, a relaxed graded epitaxial layer comprising silicon and germanium and graded with increasing germanium content at a gradient exceeding 25% Ge/μm to a final composition having a germanium content ranging from greater than 0% to 100%, wherein the structure has a threading dislocation density not exceeding $10^7/cm^2$;

a relaxed compositionally uniform cap layer disposed over the graded layer;

a p-type metal-oxide-semiconductor (PMOS) transistor disposed over the relaxed cap layer, the PMOS transistor including:

a first gate dielectric portion disposed over a first portion of the relaxed cap layer,

a first gate disposed over the first gate dielectric portion, the first gate comprising a first conducting layer,

a first source and a first drain disposed proximate the first gate dielectric portion, the first source and first drain including p-type dopants; and

an n-type metal-oxide-semiconductor (NMOS) transistor disposed over the relaxed cap layer, the NMOS transistor including:

a second gate dielectric portion disposed over a second portion of the relaxed cap layer,

a second gate disposed over the second gate dielectric portion, the second gate comprising a second conducting layer,

a second source and a second drain disposed proximate the second gate dielectric portion, the second source and second drain including n-type dopants.